

1 unit and a direct memory access unit coupled to an ATM
2 slave processing unit, the interface unit comprising:
3 an input unit, the input unit receiving data cells and
4 exchanging control signals with the ATM master processing
5 unit;
6 an input buffer unit including:
7 a buffer storage unit; and
8 a calculation unit, wherein the input buffer unit
9 receives data signals from and exchanges control signals
10 with the input unit, the input buffer unit storing received
11 data cells in the buffer storage unit, the buffer storage
12 unit transferring data cells to the ~~ATM slave processing~~
13 direct memory access unit; and
14 a register, each data cell including a cell ~~location~~
15 portion identifying a having an encoded destination
16 location, the calculation unit responsive to the contents
17 of the register and to the data cell portion for generating
18 a destination location ~~control signal~~ for the data cell in
19 the ATM slave processing unit.

20

21 2. (Original) The interface unit as recited in
22 claim 1 wherein the buffer storage unit is a first-
23 in/first-out memory unit.

24

25 **Please amend Claim 3 as follows.**

26

27 3. (Currently Amended) The interface unit as recited
28 in claim ~~1~~ 2 wherein the first-in/first-out memory unit can
29 store at least two data cells.

30

1 4. (Original) The interface unit as recited in
2 claim 1 wherein the buffer storage unit transfers a data
3 cell to the slave data processing unit every clock cycle.
4

5 **Please amend Claim 5 as follows.**
6

7 5. (Currently Amended) The interface unit as recited
8 in claim 1 wherein the destination locations can be
9 selected from at least one of the group consisting of a
10 ~~plurality of central slave~~ processing unit, a ~~plurality of~~
11 shared memory location for a plurality of slave processing
12 units, and at least one ~~central slave~~ processing unit and
13 at least one shared memory location.
14

15 **Please amend claim 6 as follows.**
16

17 6. (Currently Amended) The interface unit as recited
18 in claim 1 further comprising:

19 an output buffer unit; the output buffer unit
20 including a buffer storage unit, the buffer unit storing
21 data cells, the output buffer unit receiving data cells
22 from the ~~slave processing~~ direct memory access unit the
23 data buffer unit exchanging control signals with the slave
24 processing direct memory access unit; and

25 an output unit; the output unit receiving data cells
26 from the output buffer unit and applying data cells to the
27 ATM master processing unit, the output unit exchanging
28 control signals with the output buffer unit and with the
29 ATM master processing unit.
30

1 7. (Original) The interface unit as recited in
2 claim 1 wherein the ATM slave processing unit includes at
3 least one digital signal central processing unit.
4

5 **Please amend Claim 8 as follows.**
6

7 8. (Currently Amended) The interface unit as recited
8 in claim 1 wherein the control signals and the data cells
9 have ~~the~~ a UTOPIA format.
10

11 **Please cancel Claim 9.**
12

13 9. (Cancelled) The interface unit as recited in
14 claim 1 wherein the ATM slave processing unit includes a
15 direct memory access unit.
16

17 **Please amend claim 10 as follows.**
18

19 10. (Currently Amended) A method for exchanging data
20 cells from an ATM master processing unit with a plurality
21 of locations in an ATM slave processing unit, the ATM slave
22 processing unit including a direct memory access unit, the
23 method comprising:

24 storing data cells from the ATM master processing unit
25 in a buffer storage unit;

26 comparing a field in the data cell with the contents
27 of a register to determine the destination location of the
28 data cell;

29 generating a signal identifying the destination
30 location; and

1 when storage space is available, transferring a data
2 cell from the buffer storage unit to the ~~destination~~
3 ~~location~~ direct memory access unit.
4

5 11. (Original) The method as recited in claim 10
6 further comprising:
7 implementing the buffer storage to hold two data
8 cells; and
9 transferring a data cell from the buffer storage unit
10 to the ATM slave processing unit on consecutive clock
11 cycles.
12

13 12. (Original) The method as recited in claim 11
14 further comprising implementing the control signals in a
15 UTOPIA format.
16

17 **Please amend Claim 13 as follows.**
18

19 13. (Currently Amended) The method as recited in
20 claim 10 wherein ~~the ATM slave processing unit includes a~~
21 ~~direct memory access unit~~, the method ~~including~~ includes
22 applying the signal identifying the destination location to
23 the direct memory access unit.
24

25 **Please amend Claim 14 as follows.**
26

27 14. (Currently Amended) A data processing system
28 comprising:
29 an ATM master processing unit;

1 an ATM slave processing unit, the ATM slave processing
2 unit including a direct memory access unit; and
3 an ATM slave interface unit, the slave interface unit
4 including:
5 an input unit, the input unit receiving data
6 signals from the ATM master unit, the input unit exchanging
7 control signals with the ATM master unit;
8 an input buffer storage unit, the input buffer
9 unit including:
10 a memory unit; and
11 a calculation unit, wherein the input buffer
12 unit exchanges control signals with the input unit, the
13 input buffer unit storing data cells in the memory unit,
14 the buffer storage unit transferring data cells to the ATM
15 slave processing unit, the input buffer unit exchanging
16 control signals with the ~~ATM slave processing unit~~ direct
17 memory access unit; and
18 a register, the contents of the register
19 identifying the destination location field in a data cell,
20 the contents of the register providing the translation of
21 field in the data cell ~~to~~ into a destination location,
22 wherein the calculation unit generates a destination
23 location signal and applies the destination location signal
24 to the ATM slave processing unit.

25

26 **Please cancel Claim 15.**

27

28 15. (Cancelled) The data processing system as
29 recited in claim 14 wherein the ATM slave processing unit
30 includes a direct memory access unit, the destination

1 location signal being applied to the direct memory access
2 unit.

3

4 16. (Original) The data processing system as
5 recited in claim 14 wherein the memory unit is a first-
6 in/first-out memory unit capable of storing at least two
7 data cells.

8

9 **Please amend Claim 17 as follows.**

10

11 17. The data processing system as recited in claim 16
12 wherein the input buffer unit transfers data cells to the
13 ATM slave processing unit on consecutive ~~look~~ clock cycles.

14

15 **In the Specification**

16

17 On Page 1, please delete the Paragraph after the title.
18 Replace this Paragraph with the following Paragraph;

19

20 "This Application claims priority under 35 USC 119(e)
21 (1) of Provisional Application Serial No. 60/237,237."

22

23 On Page 1, please delete the Paragraph entitled RELATED
24 APPLICATIONS and replace this Paragraph with the following
25 Paragraph.

26

27 "This Application claims priority under 35 USC 119(e)
28 (1) of Provisional Application Serial No. 60/237,237
29 (TI-31779), titled APPARATUS AND METHOD FOR AN INTERFACE
30 UNIT FOR DATA TRANSFER BETWEEN PROCESSING UNITS IN THE